

CLAIMS

What is claimed is:

1. An Integrated Circuit (IC) device, comprising:
a first plurality of signal wires disposed within a substrate; and
a shielding mesh disposed on the substrate, the shielding mesh comprising:
a first plurality of connected wires for a first reference voltage; and
a second plurality of connected wires for a second reference voltage;
wherein at least a first portion of each of the first plurality of the signal wires
is shielded between one of the first plurality of connected wires and
one of the second plurality of connected wires from adjacent signal
wires; and
wherein a second portion of the first plurality of signal wires are adjacent to
each other in a region defined by the first and second pluralities of
connected wires.
2. An IC device as in claim 1 wherein an average length of segments of the first
and second pluralities of connected wires between nodes each of which joins more
than two wires in the shielding mesh is substantially less than an average length of
the first plurality of signal wires.
3. An IC device as in claim 1 wherein the first plurality of connected wires and

the second plurality of connected wires are in two layers in the substrate; a first plurality of vias connect the first plurality of wires; a second plurality of vias connect the second plurality of wires; and the first and second pluralities of vias divide the first and second pluralities of connected wires into segments that are substantially shorter than an average length of the first plurality of signal wires.

4. An IC device as in claim 3 wherein wires in the two layers are in directions that are in an acute angle with a direction of wires in a third layer of the IC device.

5. An IC device as in claim 4 wherein the acute angle comprises 45 degrees.

6. An IC device as in claim 3 wherein wires in the first layer are in a first direction; wires in the second layer are in a second direction; and, the first direction and the second direction are in an acute angle.

7. An IC device as in claim 6 wherein the acute angle comprises 45 degrees.

8. An IC device as in claim 1 wherein the first reference voltage is power; and the second reference voltage is ground.

9. An IC device as in claim 1 further comprising:
a second plurality of signal wires disposed within the substrate, each of the
second plurality of signal wires being shielded between two of the

first plurality of connected wires from adjacent signal lines.

10. An IC device as in claim 1 wherein a first wire of the first plurality of connected wires is wider than more than one of the first and second pluralities of connected wires.
11. An IC device as in claim 10 wherein the first wire is wider than a combined width of one of the first and second pluralities of connected wires and one of the first plurality of signal wires.
12. An IC device as in claim 1 further comprising:
a third plurality of signal wires disposed within the substrate, the third plurality of signal wires being within a window defined by a subset of the first and second pluralities of connected wires in a top view of the IC, each of the third plurality of signal wires being adjacent to at least one of the third plurality of signal wires without shielding in between.
13. An IC device as in claim 12 wherein each of the subset is substantially wider than the third plurality of signal wires.
14. An IC device as in claim 1 further comprising:
a third plurality of signal wires disposed within a first layer in the substrate, the third plurality of signal wires being within first two wires of the

first and second pluralities of connected wires, the first two wires being substantially wider than the third plurality of signal wires, the third plurality of signal wires being substantially parallel to each other, each of the third plurality of signal wires being adjacent to at least one of the third plurality of signal wires without shielding in between.

15. An IC device as in claim 14 wherein the first two wires define a first window within which signal lines are not shielded in the first layer.

16. An IC device as in claim 14 further comprising:
a fourth plurality of signal wires disposed within a second layer in the substrate, the fourth plurality of signal wires being within second two wires of the second and second pluralities of connected wires, the second two wires being substantially wider than the fourth plurality of signal wires, the fourth plurality of signal wires being substantially parallel to each other, each of the fourth plurality of signal wires being adjacent to at least one of the fourth plurality of signal wires without shielding in between.

17. An IC device as in claim 16 wherein the first two wires define a first window within which signal lines are not shielded in the first layer; the second two wires define a second window within which signal lines are not shielded in the second

layer; the first and second windows substantially coincide with each other in a top view of the IC.

18. An IC device as in claim 1 further comprising:
an IP block disposed within the substrate;
wherein first at least one of the first plurality of signal wires is a part of the
IP block; and
wherein second at least one of the first plurality of signal wires is not a part
of the IP block.
19. An IC device as in claim 18 wherein the second at least one of the first
plurality of signal wires is within a region defined by the IP block in a top view of
the IC.
20. An IC device as in claim 1 further comprising:
a first wire for the first reference voltage on a first layer of the IC device;
wherein the first plurality of connected wires comprises a second wire;
the second plurality of connected wires comprises a third wire;
the second and third wires are on the first layer of the IC device;
the first wire is between the second and third wires; and
the second and third wires are adjacent neighbors to the first wire.
21. An IC device as in claim 20 wherein spacing between the first and second

wires and between the first and third wires is substantially equal to average wire spacing in the first layer.

22. An IC device as in claim 21 wherein widths of the first, second and third wires are substantially equal.

23. An IC device as in claim 1 further comprising:
a first wire for the first reference voltage on a first layer of the IC device;
wherein the first plurality of connected wires comprises a second wire and a third wire;
the second and third wires are on the first layer of the IC device;
the first wire is between the second and third wires; and
the second and third wires are adjacent neighbors to the first wire.

24. An IC device as in claim 23 wherein spacing between the first and second wires and between the first and third wires is substantially equal to average wire spacing in the first layer.

25. An IC device as in claim 24 wherein widths of the first, second and third wires are substantially equal.

26. A method to design an Integrated Circuit (IC) device, the method comprising:

determining a representation of a shielding mesh in a substrate, the shielding mesh including a first plurality of connected wires for a first reference voltage and a second plurality of connected wires for a second reference voltage; and

routing a representation of a first plurality of signal wires in the substrate to shield at least a first portion of each of the first plurality of the signal wires between one of the first plurality of connected wires and one of the second plurality of connected wires from adjacent signal wires; wherein a second portion of the first plurality of signal wires are adjacent to each other in a region defined by the first and second pluralities of connected wires.

27. A method as in claim 26 wherein an average length of segments of the first and second pluralities of connected wires between nodes each of which joins more than two wires in the shielding mesh is substantially less than an average length of the first plurality of signal wires.

28. A method as in claim 26 wherein the first plurality of connected wires and the second plurality of connected wires are in two layers in the substrate; a first plurality of vias connect the first plurality of wires; a second plurality of vias connect the second plurality of wires; and the first and second pluralities of vias divide the first and second pluralities of connected wires into segments that are substantially shorter than an average length of the first plurality of signal wires.

29. A method as in claim 28 wherein wires in the two layers are in directions that are in an acute angle with a direction of wires in a third layer of the IC device.

30. A method as in claim 29 wherein the acute angle comprises 45 degrees.

31. A method as in claim 28 wherein wires in the first layer are in a first direction; wires in the second layer are in a second direction; and, the first direction and the second direction are in an acute angle.

32. A method as in claim 31 wherein the acute angle comprises 45 degrees.

33. A method as in claim 26 wherein the first reference voltage is power; and the second reference voltage is ground.

34. A method as in claim 26 further comprising:
routing a second plurality of signal wires in the substrate to shield each of the
second plurality of signal wires between two of the first plurality of
connected wires from adjacent signal wires.

35. A method as in claim 34 wherein the second plurality of signal wires are less subjected to signal integrity problems than the first plurality of signal wires if routed without shielding.

36. A method as in claim 26 wherein a first wire of the first plurality of connected wires is wider than more than one of the first and second pluralities of connected wires.
37. A method as in claim 36 wherein the first wire is wider than a combined width of one of the first and second pluralities of connected wires and one of the first plurality of signal wires.
38. A method as in claim 26 further comprising:
routing a third plurality of signal wires in the substrate, the third plurality of signal wires being within a window defined by a subset of the first and second pluralities of connected wires in a top view of the IC, each of the third plurality of signal wires being adjacent to at least one of the third plurality of signal wires without shielding in between.
39. A method as in claim 38 wherein each of the subset is substantially wider than the third plurality of signal wires.
40. A method as in claim 26 further comprising:
routing a third plurality of signal wires in a first layer in the substrate, the third plurality of signal wires being within first two wires of the first and second pluralities of connected wires, the first two wires being

substantially wider than the third plurality of signal wires, the third plurality of signal wires being substantially parallel to each other, each of the third plurality of signal wires being adjacent to at least one of the third plurality of signal wires without shielding in between.

41. A method as in claim 40 wherein the first two wires define a first window within which signal lines are not shielded in the first layer.

42. A method as in claim 40 further comprising:
routing a fourth plurality of signal wires in a second layer in the substrate,
the fourth plurality of signal wires being within second two wires of the second and second pluralities of connected wires, the second two wires being substantially wider than the fourth plurality of signal wires, the fourth plurality of signal wires being substantially parallel to each other, each of the fourth plurality of signal wires being adjacent to at least one of the fourth plurality of signal wires without shielding in between.

43. A method as in claim 42 wherein the first two wires define a first window within which signal lines are not shielded in the first layer; the second two wires define a second window within which signal lines are not shielded in the second layer; the first and second windows substantially coincide with each other in a top view of the IC.

44. A method as in claim 40 further comprising:
determining an allowable unshielded length of a signal line that can be
unshielded by the shielding mesh;
routing the signal line with a portion of the signal line unshielded by the
shielding mesh shorter than the allowable unshielded length.
45. A method as in claim 26 further comprising:
routing the first and second pluralities of connected wires within a region
defined by an IP block in a top view of the IC.
46. A method as in claim 26 wherein first at least one of the first plurality of
signal wires is a part of an IP block; and wherein second at least one of the first
plurality of signal wires is not a part of the IP block.
47. A method as in claim 46 wherein the second at least one of the first plurality
of signal wires is within a region defined by the IP block in a top view of the IC.
48. A method as in claim 47 further comprising:
re-routing one of the first at least one of the first plurality of signal wires.
49. A method as in claim 26 further comprising:
widening one of the first plurality of connected wires.

50. A method as in claim 49 wherein said widening comprises:
combining at least two of adjacent ones of the first plurality of connected
wires into one wider wire.
51. A method as in claim 49 wherein said widening comprises:
filling in an area between two of the first plurality of connected wires to
generate one wider wire.
52. A method as in claim 26 further comprising:
routing a first wire for the first reference voltage on a first layer of the IC
device;
wherein the first plurality of connected wires comprises a second wire;
the second plurality of connected wires comprises a third wire;
the second and third wires are on the first layer of the IC device;
the first wire is between the second and third wires; and
the second and third wires are adjacent neighbors to the first wire.
53. A method as in claim 52 wherein spacing between the first and second wires
and between the first and third wires is substantially equal to average wire spacing in
the first layer.
54. A method as in claim 53 wherein widths of the first, second and third wires

are substantially equal.

55. A method as in claim 26 further comprising:
routing a first wire for the first reference voltage on a first layer of the IC device;
wherein the first plurality of connected wires comprises a second wire and a third wire;
the second and third wires are on the first layer of the IC device;
the first wire is between the second and third wires; and
the second and third wires are adjacent neighbors to the first wire.

56. A method as in claim 55 wherein spacing between the first and second wires and between the first and third wires is substantially equal to average wire spacing in the first layer.

57. A method as in claim 56 wherein widths of the first, second and third wires are substantially equal.

58. A machine readable medium containing executable computer program instructions which when executed by a digital processing system cause said system to perform a method to design an Integrated Circuit (IC) device, the method comprising:

determining a representation of a shielding mesh in a substrate, the shielding mesh including a first plurality of connected wires for a first reference voltage and a second plurality of connected wires for a second reference voltage; and

routing a representation of a first plurality of signal wires in the substrate to shield at least a first portion of each of the first plurality of the signal wires between one of the first plurality of connected wires and one of the second plurality of connected wires from adjacent signal wires;

wherein a second portion of the first plurality of signal wires are adjacent to each other in a region defined by the first and second pluralities of connected wires.

59. A medium as in claim 58 wherein an average length of segments of the first and second pluralities of connected wires between nodes each of which joins more than two wires in the shielding mesh is substantially less than an average length of the first plurality of signal wires.

60. A medium as in claim 58 wherein the first plurality of connected wires and the second plurality of connected wires are in two layers in the substrate; a first plurality of vias connect the first plurality of wires; a second plurality of vias connect the second plurality of wires; and the first and second pluralities of vias divide the first and second pluralities of connected wires into segments that are substantially shorter than an average length of the first plurality of signal wires.

61. A medium as in claim 60 wherein wires in the two layers are in directions that are in an acute angle with a direction of wires in a third layer of the IC device.
62. A medium as in claim 61 wherein the acute angle comprises 45 degrees.
63. A medium as in claim 60 wherein wires in the first layer are in a first direction; wires in the second layer are in a second direction; and, the first direction and the second direction are in an acute angle.
64. A medium as in claim 63 wherein the acute angle comprises 45 degrees.
65. A medium as in claim 58 wherein the first reference voltage is power; and the second reference voltage is ground.
66. A medium as in claim 58 wherein the method further comprises:
routing a second plurality of signal wires in the substrate to shield each of the
second plurality of signal wires between two of the first plurality of
connected wires from adjacent signal wires.
67. A medium as in claim 66 wherein the second plurality of signal wires are less subjected to signal integrity problems than the first plurality of signal wires if routed without shielding.

68. A medium as in claim 58 wherein a first wire of the first plurality of connected wires is wider than more than one of the first and second pluralities of connected wires.

69. A medium as in claim 68 wherein the first wire is wider than a combined width of one of the first and second pluralities of connected wires and one of the first plurality of signal wires.

70. A medium as in claim 58 wherein the method further comprises:
routing a third plurality of signal wires in the substrate, the third plurality of signal wires being within a window defined by a subset of the first and second pluralities of connected wires in a top view of the IC, each of the third plurality of signal wires being adjacent to at least one of the third plurality of signal wires without shielding in between.

71. A medium as in claim 70 wherein each of the subset is substantially wider than the third plurality of signal wires.

72. A medium as in claim 58 wherein the method further comprises:
routing a third plurality of signal wires in a first layer in the substrate, the third plurality of signal wires being within first two wires of the first and second pluralities of connected wires, the first two wires being

substantially wider than the third plurality of signal wires, the third plurality of signal wires being substantially parallel to each other, each of the third plurality of signal wires being adjacent to at least one of the third plurality of signal wires without shielding in between.

73. A medium as in claim 72 wherein the first two wires define a first window within which signal lines are not shielded in the first layer.

74. A medium as in claim 72 wherein the method further comprises:
routing a fourth plurality of signal wires in a second layer in the substrate,
the fourth plurality of signal wires being within second two wires of the second and second pluralities of connected wires, the second two wires being substantially wider than the fourth plurality of signal wires, the fourth plurality of signal wires being substantially parallel to each other, each of the fourth plurality of signal wires being adjacent to at least one of the fourth plurality of signal wires without shielding in between.

75. A medium as in claim 74 wherein the first two wires define a first window within which signal lines are not shielded in the first layer; the second two wires define a second window within which signal lines are not shielded in the second layer; the first and second windows substantially coincide with each other in a top view of the IC.

76. A medium as in claim 72 wherein the method further comprises:
determining an allowable unshielded length of a signal line that can be
unshielded by the shielding mesh;
routing the signal line with a portion of the signal line unshielded by the
shielding mesh shorter than the allowable unshielded length.
77. A medium as in claim 58 wherein the method further comprises:
routing the first and second pluralities of connected wires within a region
defined by an IP block in a top view of the IC.
78. A medium as in claim 58 wherein first at least one of the first plurality of
signal wires is a part of an IP block; and wherein second at least one of the first
plurality of signal wires is not a part of the IP block.
79. A medium as in claim 78 wherein the second at least one of the first plurality
of signal wires is within a region defined by the IP block in a top view of the IC.
80. A medium as in claim 79 wherein the method further comprises:
re-routing one of the first at least one of the first plurality of signal wires.
81. A medium as in claim 58 wherein the method further comprises:
widening one of the first plurality of connected wires.

82. A medium as in claim 81 wherein said widening comprises:
combining at least two of adjacent ones of the first plurality of connected
wires into one wider wire.
83. A medium as in claim 81 wherein said widening comprises:
filling in an area between two of the first plurality of connected wires to
generate one wider wire.
84. A medium as in claim 58 wherein the method further comprises:
routing a first wire for the first reference voltage on a first layer of the IC
device;
wherein the first plurality of connected wires comprises a second wire;
the second plurality of connected wires comprises a third wire;
the second and third wires are on the first layer of the IC device;
the first wire is between the second and third wires; and
the second and third wires are adjacent neighbors to the first wire.
85. A medium as in claim 84 wherein spacing between the first and second wires
and between the first and third wires is substantially equal to average wire spacing in
the first layer.
86. A medium as in claim 85 wherein widths of the first, second and third wires

are substantially equal.

87. A medium as in claim 58 wherein the method further comprises:
routing a first wire for the first reference voltage on a first layer of the IC
device;
wherein the first plurality of connected wires comprises a second wire and a
third wire;
the second and third wires are on the first layer of the IC device;
the first wire is between the second and third wires; and
the second and third wires are adjacent neighbors to the first wire.

88. A medium as in claim 87 wherein spacing between the first and second wires
and between the first and third wires is substantially equal to average wire spacing in
the first layer.

89. A medium as in claim 88 wherein widths of the first, second and third wires
are substantially equal.

90. A method of designing an integrated circuit (IC), said method comprising:
creating a representation of a shielding mesh in a representation of a design
of said IC, said shielding mesh comprising a first single layer
shielding mesh and a first double layer shielding mesh which is
coupled to said first single layer shielding mesh;

creating a representation of a first signal line having a first unshielded portion, which is disposed in a first region of said IC which is adjacent to said first single layer shielding mesh, and having a first shielded portion which is disposed in said first single layer shielding mesh, and having a second shielded portion which is disposed in said first double layer shielding mesh.

91. A method as in claim 90 wherein said first signal line also comprises a third shielded portion which is disposed in a second single layer shielding mesh and a second unshielded portion which is disposed in a second region of said IC which is adjacent to said second single layer shielding mesh.

92. A method as in claim 91 wherein said creating said representation of said first signal line comprises routing said first unshielded portion to said first single layer shielding mesh, routing said first shielded portion in said first single layer shielding mesh, routing said second shielded portion in said first double layer shielding mesh, routing said third shielded portion in said second single layer shielding mesh, and routing said second unshielded portion to said second region.

93. A method as in claim 92 wherein said shielding mesh comprises a second double layer shielding mesh which is coupled to said second single layer shielding mesh and wherein said first signal line comprises a fourth shielded portion which is disposed in said second double layer shielded mesh.

94. A method as in claim 91 wherein each of said first single layer shielding mesh, said first double layer shielding mesh, and said second single layer shielding mesh comprises a first plurality of reference voltage lines designed to provide a first reference voltage and a second plurality of reference voltage lines designed to provide a second reference voltage.

95. A method as in claim 94, said method further comprising:
creating a representation of at least one reference voltage line, designed to provide said first reference voltage, disposed between a pair of adjacent second plurality of reference voltage lines in said shielding mesh.

96. A method as in claim 95, wherein said at least one reference voltage line provides a bypass capacitance between said first and said second reference voltages and is created after signal lines have been routed in said shielding mesh.

97. A machine readable medium containing executable computer program instructions which when executed by a digital processing system cause said system to perform a method of designing an integrated circuit (IC), said method comprising:
creating a representation of a shielding mesh in a representation of a design of said IC, said shielding mesh comprising a first single layer shielding mesh and a first double layer shielding mesh which is

coupled to said first single layer shielding mesh;
creating a representation of a first signal line having a first unshielded portion, which is disposed in a first region of said IC which is adjacent to said first single layer shielding mesh, and having a first shielded portion which is disposed in said first single layer shielding mesh, and having a second shielded portion which is disposed in said first double layer shielding mesh.

98. A machine readable medium as in claim 97 wherein said first signal line also comprises a third shielded portion which is disposed in a second single layer shielding mesh and a second unshielded portion which is disposed in a second region of said IC which is adjacent to said second single layer shielding mesh.

99. A machine readable medium as in claim 98 wherein said creating said representation of said first signal line comprises routing said first unshielded portion to said first single layer shielding mesh, routing said first shielded portion in said first single layer shielding mesh, routing said second shielded portion in said first double layer shielding mesh, routing said third shielded portion in said second single layer shielding mesh, and routing said second unshielded portion to said second region.

100. A machine readable medium as in claim 99 wherein said shielding mesh comprises a second double layer shielding mesh which is coupled to said second

single layer shielding mesh and wherein said first signal line comprises a fourth shielded portion which is disposed in said second double layer shielded mesh.

101. A machine readable medium as in claim 98 wherein each of said first single layer shielding mesh, said first double layer shielding mesh, and said second single layer shielding mesh comprises a first plurality of reference voltage lines designed to provide a first reference voltage and a second plurality of reference voltage lines designed to provide a second reference voltage.

102. A machine readable medium as in claim 101, said method further comprising:

creating a representation of at least one reference voltage line, designed to provide said first reference voltage, disposed between a pair of adjacent second plurality of reference voltage lines in said shielding mesh.

103. A machine readable medium as in claim 102, wherein said at least one reference voltage line provides a bypass capacitance between said first and said second reference voltages and is created after signal lines have been routed in said shielding mesh.

104. An integrated circuit (IC) device comprising:

a shielding mesh having at least a first portion disposed in a first layer of said

IC and at least a second portion disposed in said first layer and a second layer, wherein said shielding mesh comprises a first single layer shielding mesh and a first double layer shielding mesh which is coupled to said first single layer shielding mesh;

at least a first signal line having a first unshielded portion, which is disposed in a first region of said IC which is adjacent to said first single layer shielding mesh, and having a first shielded portion which is disposed in said first single layer shielding mesh, and having a second shielded portion which is disposed in said first double layer shielding mesh.

105. An IC as in claim 104 wherein said first signal line also comprises a third shielded portion which is disposed in a second single layer shielding mesh and a second unshielded portion which is disposed in a second region of said IC which is adjacent to said second single layer shielding mesh.

106. An IC as in claim 105 wherein said shielding mesh comprises a second double layer shielding mesh which is coupled to said second single layer shielding mesh and wherein said first signal line comprises a fourth shielded portion which is disposed in said second double layer shielded mesh.

107. An IC as in claim 105 wherein each of said first single layer shielding mesh, said first double layer shielding mesh, and said second single layer shielding mesh comprises a first plurality of reference voltage lines designed to provide a first

reference voltage and a second plurality of reference voltage lines designed to provide a second reference voltage.

108. An IC as in claim 107, further comprising:

at least one reference voltage line, designed to provide said first reference voltage, disposed between a pair of adjacent second plurality of reference voltage lines in said shielding mesh.

109. An IC as in claim 108, wherein said at least one reference voltage line provides a bypass capacitance between said first and said second reference voltages.

110. A method of designing an integrated circuit (IC), said method comprising:

creating a representation of a shielding mesh in at least one layer of a representation of a design of said IC;

routing representations of signal lines in said shielding mesh and outside of said shielding mesh based upon a set of predetermined rules;

determining whether a re-routing condition exists;

identifying removable shielding lines in said shielding mesh in response to determining that said re-routing condition exists.

111. A method as in claim 110, wherein said method further comprises:

routing representations of signal lines in place of removable shielding lines,

and wherein said shielding mesh comprises at least two layers of said

IC, and wherein said re-routing condition exists if there are insufficient routing resources or if a routing exceeds a timing requirement.

112. A method as in claim 110, wherein said method further comprises:
routing additional reference voltage lines in said shielding mesh to provide
for bypass capacitors.
113. A method as in claim 110 wherein said shielding mesh comprises at least one window having a lower shielding density than said shielding mesh.
114. A method as in claim 110, wherein said method further comprises:
determining a maximum unshielded line length for at least some of said
signal lines;
routing at least a first signal line in an unshielded manner if said first signal
line has a length which is less than said maximum unshielded line
length for said first signal line.
115. A method as in claim 110, wherein said predetermined rules comprise at least one of: (a) routing long signal lines between opposite reference voltage lines in said shielding mesh; (b) routing noisy signal lines between opposite reference voltage lines in said shielding mesh; (c) routing clock lines in said shielding mesh; (d) routing signal lines, which have a length which exceed their calculated maximum

unshielded line length, in said shielding mesh; (e) routing signal lines which transition between states at near the same time as a clock signal transitions between states in said shielding mesh; or (f) routing signal lines, which are not directly connected to circuitry in a predesigned block of logic, over said predesigned block of logic through an integral shielding mesh of said predesigned block of logic.

116. A machine readable medium containing executable computer program instructions which when executed by a digital processing system cause said system to perform a method of designing an integrated circuit (IC), said method comprising:

- creating a representation of a shielding mesh in at least one layer of a representation of a design of said IC;
- routing representations of signal lines in said shielding mesh and outside of said shielding mesh based upon a set of predetermined rules;
- determining whether a re-routing condition exists;
- identifying removable shielding lines in said shielding mesh in response to determining that said re-routing condition exists.

117. A machine readable medium as in claim 116, wherein said method further comprises:

- routing representations of signal lines in place of removable shielding lines, and wherein said shielding mesh comprises at least two layers of said IC, and wherein said re-routing condition exists if there are insufficient routing resources or if a routing exceeds a timing

requirement.

118. A machine readable medium as in claim 116, wherein said method further comprises:

routing additional reference voltage lines in said shielding mesh to provide for bypass capacitors.

119. A machine readable medium as in claim 116 wherein said shielding mesh comprises at least one window having a lower shielding density than said shielding mesh.

120. A machine readable medium as in claim 116, wherein said method further comprises:

determining a maximum unshielded line length for at least some of said signal lines;

routing at least a first signal line in an unshielded manner if said first signal line has a length which is less than said maximum unshielded line length for said first signal line.

121. A machine readable medium as in claim 116, wherein said predetermined rules comprise at least one of: (a) routing long signal lines between opposite reference voltage lines in said shielding mesh; (b) routing noisy signal lines between opposite reference voltage lines in said shielding mesh; (c) routing clock lines in

said shielding mesh; (d) routing signal lines, which have a length which exceed their calculated maximum unshielded line length, in said shielding mesh; (e) routing signal lines which transition between states at near the same time as a clock signal transitions between states in said shielding mesh; or (f) routing signal lines, which are not directly connected to circuitry in a predesigned block of logic, over said predesigned block of logic through an integral shielding mesh of said predesigned block of logic.

122. A method of designing an integrated circuit (IC), said method comprising:
- creating a representation of a shielding mesh in at least one layer of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage, said shielding mesh having a plurality of gaps between said first and said second plurality of lines;
 - routing a representation of at least one signal line in said plurality of gaps;
 - determining whether a gap from said plurality of gaps remains in said IC after said routing;
 - increasing a representation of an amount of a conductive material of at least one of said first and said second plurality of lines in response to said determining.

123. A method as in claim 122 wherein at least two of said first plurality of lines

and at least two of said second plurality of lines have portions which are parallel and wherein adjacent lines of said portions are separated by a distance of less than about 1 micron.

124. A method as in claim 122 wherein said increasing comprises increasing a width of said at least one of said first and said second plurality of lines.

125. A method as in claim 124 wherein said increasing comprises adding an additional line providing one of said first reference voltage or said second reference voltage.

126. A method as in claim 124 wherein each of said at least two of said first plurality of lines and each of said at least two of said second plurality of lines have a width of less than 3 microns prior to said increasing said width.

127. An integrated circuit (IC) device comprising:

a shielding mesh in at least one layer of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage, at least one of said first plurality of lines and said second plurality of lines being wider than other lines of said first and said second plurality of lines;

at least one signal line disposed in said at least one layer between two of said

first and said second plurality of lines.

128. An IC as in claim 127 wherein at least two of said first plurality of lines and at least two of said second plurality of lines have portions which are parallel and wherein adjacent lines of said portions are separated by a distance of less than about 1 micron.

129. An IC as in claim 127 wherein said shielding mesh comprises at least two layers having said first and said second plurality of lines.

130. An IC as in claim 129 wherein all of said lines of said first plurality of lines and said second plurality of lines are less than about 5 microns in width.

131. A method of designing an integrated circuit (IC), said method comprising:
incorporating a representation of a predesigned block of logic having at least one integral shielding layer in a representation of a design of an IC having at least one additional block;
routing at least one signal line from said at least one additional block through said at least one integral shielding layer.

132. A method as in claim 131 wherein said predesigned block of logic has a plurality of design information which may not be available to a second IC owner which is responsible for said designing of said IC and wherein said predesigned

block of logic was designed by a first IC owner which controls access to said plurality of design information.

133. A method as in claim 131 wherein said predesigned block of logic is completely designed and laid out such that it can be taped out for a semiconductor fabrication process.

134. A method as in claim 133 wherein said at least one integral shielding layer comprises at least two shielding layers.

135. A method as in claim 131 wherein said at least one integral shielding layer comprises a first plurality of lines which are designed to provide a first reference voltage and a second plurality of lines which are designed to provide a second reference voltage and wherein said first plurality and said second plurality of lines are arranged in a substantially interleaved manner and are substantially parallel over at least a portion of their lengths.

136. A method as in claim 135 wherein a portion of at least four lines of said first plurality of lines and a portion of at least four lines of said second plurality of lines are disposed in an area of less than about 50 microns by 50 microns and wherein said at least one signal line is not directly connected to circuitry in said predesigned block of logic.

137. A method as in claim 136 wherein a plurality of signal lines are routed between adjacent pairs of said first and second plurality of lines and wherein said at least one additional block comprises a first additional block and a second additional block and wherein said plurality of signal lines are routed through said at least one shielding layer from said first additional block to said second additional block.

138. An integrated circuit (IC) device comprising:
a predesigned block of logic in said IC, said predesigned block of logic
having an integral shielding layer;
at least one signal line from an additional block of logic, said at least one
signal line being routed through said integral shielding layer.

139. An IC as in claim 138 wherein said predesigned block of logic has a plurality of design information which may not be available to a second designer which designed said IC and wherein said predesigned block of logic was designed by a first designer which controls access to said plurality of design information.

140. An IC as in claim 139 wherein said at least one signal line is not directly connected to circuitry in said predesigned block of logic.

141. An IC as in claim 140 wherein said integral shielding layer comprises a first plurality of lines which are designed to provide a first reference voltage and a second plurality of lines which are designed to provide a second reference voltage,

and wherein said first plurality and said second plurality of lines are arranged in a substantially interleaved manner and are parallel along at least a portion of their lengths.

142. An IC as in claim 141 wherein a portion of at least four lines of said first plurality of lines and a portion of at least four lines of said second plurality of lines are disposed in an area of less than about 50 microns by 50 microns.

143. An IC as in claim 142 wherein a plurality of signal lines are disposed between adjacent pairs of said first and said second plurality of lines and wherein said plurality of signal lines are routed through said integral shielding layer from said additional block to another additional block.

144. A method of designing an integrated circuit (IC), said method comprising:
creating a representation of at least a first layer and a second layer having
conductive lines which are routed substantially orthogonally relative
to a first reference axis and a second reference axis;
creating a representation of at least two additional layers which comprise a
shielding mesh which comprises lines routed substantially non-
orthogonally relative to said first and said second reference axes.

145. A method as in claim 144 wherein said conductive lines in said first layer and in said second layer are substantially perpendicular to one of said first and said

second reference axes, and wherein said lines in said shielding mesh are at an angle in a range of about 30° to 60° relative to one of said first and said second reference axes.

146. A method as in claim 144 wherein said first reference axis is parallel to a representation of a first edge of said IC and said second reference axis is parallel to a representation of a second edge of said IC.

147. A method as in claim 146 wherein said shielding mesh comprises a first plurality of lines which are designed to provide a first reference voltage and a second plurality of lines which are designed to provide a second reference voltage and wherein at least a portion of said first plurality of lines and a portion of said second plurality of lines are parallel.

148. A method as in claim 147 wherein a portion of at least four lines of said first plurality of lines and a portion of at least four lines of said second plurality of lines are disposed in an area of less than about 50 microns by 50 microns.

149. A method as in claim 148 wherein said shielding mesh comprises at least one window.

150. A method as in claim 147 wherein a representation of a plurality of signal lines are routed through said shielding mesh on said at least two additional layers.

151. An integrated circuit (IC) comprising:

at least a first layer and a second layer having conductive lines which are routed substantially orthogonally relative to a first reference axis and a second reference axis;

at least two additional layers which comprise a shielding mesh which comprises lines routed substantially non-orthogonally relative to said first and said second reference axes.

152. An IC as in claim 151 wherein said conductive lines in said first layer and in said second layer are substantially perpendicular to one of said first and said second reference axes, and wherein said lines in said shielding mesh are at an angle in a range of about 30° to 60° relative to one of said first and said second reference axes.

153. An IC as in claim 151 wherein said first reference axis is parallel to a first edge of said IC and said second reference axis is parallel to a second edge of said IC.

154. An IC as in claim 153 wherein said shielding mesh comprises a first plurality of lines which are designed to provide a first reference voltage and a second plurality of lines which are designed to provide a second reference voltage and wherein at least a portion of said first plurality of lines and a portion of said second plurality of lines are parallel.

155. An IC as in claim 154 wherein a portion of at least four lines of said first plurality of lines and a portion of at least four lines of said second plurality of lines are disposed in an area of less than about 50 microns by 50 microns.

156. An IC as in claim 155 wherein said shielding mesh comprises at least one window.

157. An IC as in claim 154 wherein a plurality of signal lines are routed through said shielding mesh on said at least two additional layers.

158. A method of designing an integrated circuit (IC), said method comprising:
generating a representation of a shielding mesh in at least one layer of a representation of a design of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage and having a first density of lines determined by a number of said first plurality and said second plurality of lines within a given area of said shielding mesh;
determining a congestion level of signal lines in a computer aided IC design process;
creating, in response to said determining said congestion level, a representation of a window in said shielding mesh, said window having a second density of lines which provide either said first

reference voltage or said second reference voltage, said second density being less than said first density;
routing representations of signal lines in said window.

159. A method as in claim 158 wherein said second density is zero.

160. A method as in claim 158 wherein said second density is greater than zero and less than said first density.

161. A method as in claim 160 wherein at least some of said signal lines in said window are adjacent to at least one line of said first plurality or said second plurality of lines.

162. A method as in claim 160 wherein said window constitutes a space made available for a signal line by replacing one of said first or said second plurality of lines in said shielding mesh with said signal line.

163. A method as in claim 158 wherein said window is bordered by at least two sides of said shielding mesh.

164. A method as in claim 163 wherein said window is bordered by only two sides of said shielding mesh.

165. A method as in claim 158 wherein said design is represented in a machine readable format which is stored in a storage device and is used in a computer aided design process.

166. A method as in claim 158 wherein at least two of said first plurality of lines and at least two of said second plurality of lines have portions which are parallel and wherein adjacent lines of said portions are separated by a distance of less than about 1 micron.

167. A method as in claim 158 wherein said shielding mesh comprises at least two layers.

168. A method as in claim 167 wherein each signal line which is routed in said window is determined to be safely routed in said window through a signal integrity analysis.

169. An integrated circuit (IC) device comprising:
at least one layer having a shielding mesh which comprises a first plurality of lines which are designed to provide a first reference voltage and a second plurality of lines which are designed to provide a second reference voltage and having a first density of lines determined by a number of said first plurality of lines and said second plurality of lines within a given area of said shielding mesh, said shielding mesh

a window which has a second density of lines which provide either said first reference voltage or said second reference voltage, said second density being less than said first density;
at least one signal line routed in said window.

170. An IC as in claim 169 wherein said second density is zero.

171. An IC as in claim 169 wherein said second density is greater than zero and less than said first density.

172. An IC as in claim 171 wherein at least some of said signal lines in said window are adjacent to at least one line of said first plurality or said second plurality of lines.

173. An IC as in claim 171 wherein said window constitutes a space made available for a signal line by replacing, in a design process, one of said first or said second plurality of lines in said shielding mesh with said signal line.

174. An IC as in claim 169 wherein said window is bordered by at least two sides of said shielding mesh.

175. An IC as in claim 174 wherein said window is bordered by only two sides of said shielding mesh.

176. An IC as in claim 169 wherein at least two of said first plurality of lines and at least two of said second plurality of lines have portions which are parallel and wherein adjacent lines of said portions are separated by a distance of less than about 1 micron.

177. An IC as in claim 169 wherein said shielding mesh comprises at least two layers.

178. An IC as in claim 177 wherein each signal which is routed in said window is determined to be safely routed in said window through a signal integrity analysis.

179. A method of designing an integrated circuit (IC), said method comprising:
generating a representation of a shielding mesh in at least one layer of a representation of a design of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage and having a first density of lines determined by a number of said first plurality and said second plurality of lines within a given area of said shielding mesh;
creating a representation of a window in said shielding mesh, said window having a second density of lines which provide either said first reference voltage or said second reference voltage, said second

density being less than said first density;

creating a representation of at least one signal line disposed in said window.

180. A method as in claim 179 wherein said second density is zero.

181. A method as in claim 179 wherein said second density is greater than zero.

182. A method as in claim 181 wherein said at least one signal line in said window is adjacent to at least one line of said first plurality or said second plurality of lines.

183. A method of designing an integrated circuit (IC), said method comprising:
determining a desired amount of decoupling capacitance in a representation
of a design of an IC;
routing signal lines in at least one layer of a shielding mesh of said
representation of said design, said routing taking into account said
desired amount to provide a preserved space in said shielding mesh
for decoupling lines;
routing capacitive decoupling lines in said shielding mesh, thereby using at
least some of said preserved space.

184. A method as in claim 183 wherein a portion of a total of available routing resources for routing signal lines is not used in said routing, said portion

corresponding to said amount of decoupling capacitance.

185. A method as in claim 183 wherein said shielding mesh comprises a first plurality of lines which are designed to provide a first reference voltage and a second plurality of lines which are designed to provide a second reference voltage and wherein at least two of said first plurality of lines and at least two of said second plurality of lines have portions which are parallel and wherein adjacent lines of said portions are separated by a distance of less than about 1 micron.

186. A method as in claim 183 wherein other signal lines are not routed in said shielding mesh as a result of a signal integrity analysis for said other signal lines.

187. A method as in claim 183 wherein said representation of said design is stored in a machine readable format in a storage device and is used in a computer aided design process.

188. A method of designing an integrated circuit (IC), said method comprising:
creating a representation, in at least one layer of said IC, of a shielding mesh of lines having a first plurality of lines designed to provide a first reference voltage and a second plurality of lines designed to provide a second reference voltage;
adding a representation of at least one line, providing one of either said first reference voltage or said second reference voltage, which is

positioned adjacent to a line providing the other of said first and said second reference voltage.

189. A method as in claim 188 wherein decoupling capacitance is provided by said shielding mesh.

190. A method as in claim 188 further comprising:
routing a representation of at least one signal line through at least a portion of said shielding mesh.

191. An integrated circuit (IC) device comprising:
at least one layer in said IC having a shielding mesh which comprises a first plurality of lines designed to provide a first reference voltage and a second plurality of lines designed to provide a second reference voltage, said shielding mesh having a density of at least a portion of 10 lines which provide one of said reference voltages in an area of about 50 microns by 25 microns;
a plurality of signal lines routed through said shielding mesh, each of said signal lines being disposed adjacent to at least one of said first plurality or said second plurality of lines, wherein at least one of said first plurality of lines and at least one of said second plurality of lines are adjacent to each other, without a signal line intervening, to provide a capacitance coupling between them.

192. An IC as in claim 191 wherein a distance of less than about 10 microns separates one of said first plurality of lines from a neighboring one of said second plurality of lines.

193. An IC as in claim 191 wherein a width of each of said lines of said first plurality of lines and said second plurality of lines is less than about 3 microns.

194. An IC as in claim 191 wherein said capacitance coupling acts as an intentionally included bypass capacitor coupled between said first reference voltage and said second reference voltage.

195. A method of designing an integrated circuit (IC), said method comprising:
creating a representation of at least one layer of said IC, said at least one layer having a mesh which comprises a repeating pattern of at least two adjacent first plurality of lines and at least two adjacent second plurality of lines, said first plurality of lines designed to provide a first reference voltage and said second plurality of lines designed to provide a second reference voltage;
creating a representation of at least one line, designed to provide said first reference voltage, disposed between a pair of adjacent second plurality of lines.

196. A method as in claim 195 further comprising:

modifying said representation of said at least one layer to include at least one signal line routed adjacent to at least one of said first or said second plurality of lines on said at least one layer.

197. A method as in claim 195 further comprising:

modifying said representation of said at least one layer to include a first plurality of signal lines each routed between an adjacent pair of one of said first plurality of lines and one of said second plurality of lines on said at least one layer;

modifying said representation of said at least one layer to include a second plurality of signal lines each routed between an adjacent pair of (a) said first plurality of lines or (b) said second plurality of lines.

198. A method as in claim 196 wherein said mesh is a shielding mesh and wherein said representation of said at least one layer is stored in a machine readable format in a storage device which is used in a computer aided design process.

199. A method as in claim 198 wherein said shielding mesh has a density of at least ten lines of said first and said second plurality of lines in an area of about 50 microns by 25 microns.

200. A method as in claim 197 wherein said mesh has a density of at least ten lines of said first and said second plurality of lines in an area of about 50 microns by

25 microns.

201. A method of designing an integrated circuit (IC), said method comprising:
creating a representation of at least one layer of said IC, said at least one layer having a repeating pattern of at least two adjacent first plurality of lines and at least two adjacent second plurality of lines, said first plurality of lines designed to provide a first reference voltage and said second plurality of lines designed to provide a second reference voltage;
creating a representation of at least one signal line disposed adjacent to at least one of said first or said second plurality of lines on said at least one layer.

202. A method as in claim 201 wherein each of a plurality of signal lines are disposed between one of (a) two adjacent first plurality of lines; (b) two adjacent second plurality of lines; or (c) a pair adjacent of a line of said first plurality of lines and a line of said second plurality of lines.

203. A method as in claim 202 wherein said repeating pattern is a shielding mesh and wherein said representation of said at least one layer is stored in a machine readable format in a storage device which is used in a computer aided design process.

204. A method as in claim 203 wherein said shielding mesh has a density of at least ten lines of said first and said second plurality of lines in an area of about 50 microns by 25 microns.

205. A method as in claim 201 further comprising:
creating a representation of at least one additional line designed to carry said first reference voltage, said at least one additional line being routed between an adjacent pair of lines of said second plurality of lines.

206. A method as in claim 205 wherein said additional line creates a decoupling capacitor between itself and said adjacent pair of lines.

207. An IC as in claim 104 wherein said first double layer shielding mesh is in a first layer and a second layer of said IC and wherein at least a first portion of said first single layer shielding mesh is in one of said first and said second layers and wherein at least a second portion of said first single layer shielding mesh is in a third layer of said IC.